Honeywell

ESCAN

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Outline

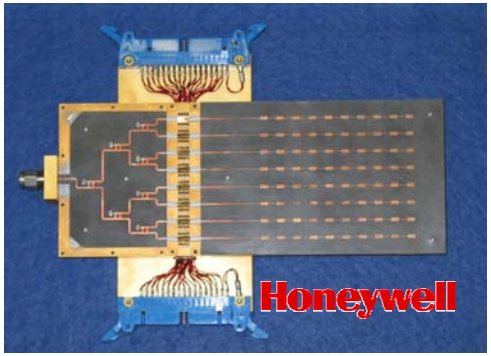
- **Reconfigurable Antennas**
  - Nomenclature… What is Reconfigurable?
  - Benefits
- **ESCAN**
  - Design
  - Program Goals
  - ASIC Development
    - RF Switch Performance
    - Photocell Performance
  - Production Cost
  - Required Steps in Array Fabrication & Measurement

Reconfigurable Array

- Reconfigurable apertures are distinguished from other types of traditional electronic antennas by their ability to alter the current distribution through their aperture. A reconfigurable array is capable of changing its element pattern and complex array factor.[1]

Fixed element pattern of Phased Array

$$\vec{E} = \frac{j\omega\mu_o e^{-jk\vec{r}_o}}{\vec{r}_o} f_e(\theta,\phi)\sum_{1}^{N} a_i e^{-jk(\hat{r}\cdot\vec{r}_i)}$$



Electronically Steered Phased Array

Reconfigurable Element Pattern

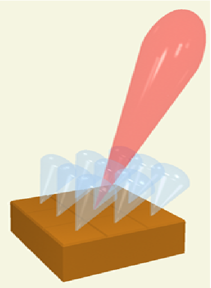
$$\vec{E} = \frac{j\omega\mu_o e^{-jk\vec{r}_o}}{\vec{r}_o} \sum_{1}^{N} f_i(\theta,\phi) a_i e^{-jk(\hat{r}\cdot\vec{r}_i)}$$

E. R. Brown, "On the Gain of a Reconfigurable-Aperture Antenna", IEEE Trans. Antennas Propagat., vol AP-49, pp. 1357, Oct. 2001.

Basic Features of Reconfigurable Elements

- **A Structural Design that Enables the Radiator to Electrically Evolve**
  - High capacity to vary element shape and resonant length scales
    - Antennas that switch a limited number of radiators in and out are often referred to as "Smart or Adaptive" and have more restricted performance
  - A design which allows for broadband impedance matching capability
    - Maximizes bandwidth and gain
    - Improves beam steering capability with a single feed
- **Embedded Control Electronics**
  - Deliver power and reconfiguration instruction into the aperture
  - Minimize electromagnetic interference with the radiative function (no conductive wires)
  - Maintain the current distribution integrity through the aperture
  - Enable fast reconfiguration times
    - Facilitates tracking

Benefits of Reconfigurable Elements/Arrays

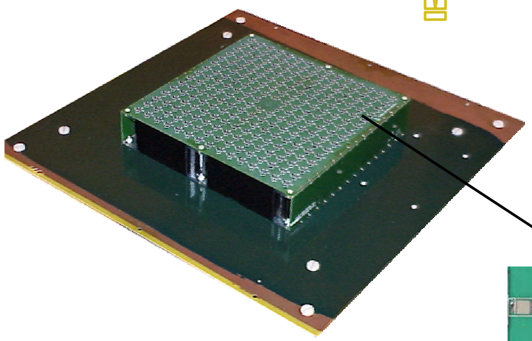


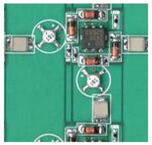
Reconfigurable Aperture

- **Multifunctional Aperture**
  - Possesses weight, cost, and signature reduction benefits
- **Adapts to the External Communication Environment**
  - Null steering for anti-jamming capability
  - Enables gain for bandwidth trades
- **Single Feed Steering**
  - Reconfigurable structures permit steering at frequencies above the grating lobes without the immediate loss in gain experienced in phased array concepts.
- **Low Observables**
  - During periods when the antenna functionality is not required the reconfigurability of the aperture may be utilized to force the structure to function as R-card for signature reduction.

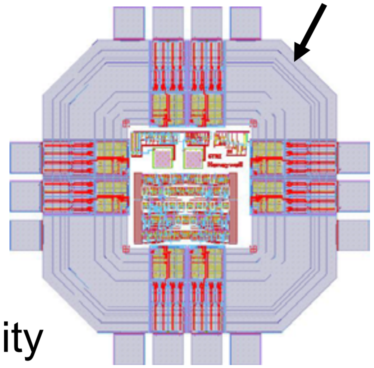
ESCAN: 800MHz-2.6GHz 5x1 Reconfigurable Array

- **Structural Form of the Element**
  - Utilizes a proven reconfigurable element concept developed at Georgia Tech (GTRI)[2]
  - Funded by DARPA RECAP/ FCS-C Programs
    - **GTRI RECAP** Bandwidth: 500MHz-2.7GHz
    - **GTRI RECAP** Directive Gain: 14dB (1.3λ X 1.3λ)
    - **GTRI RECAP** Beamsteer: +/-55^{o}





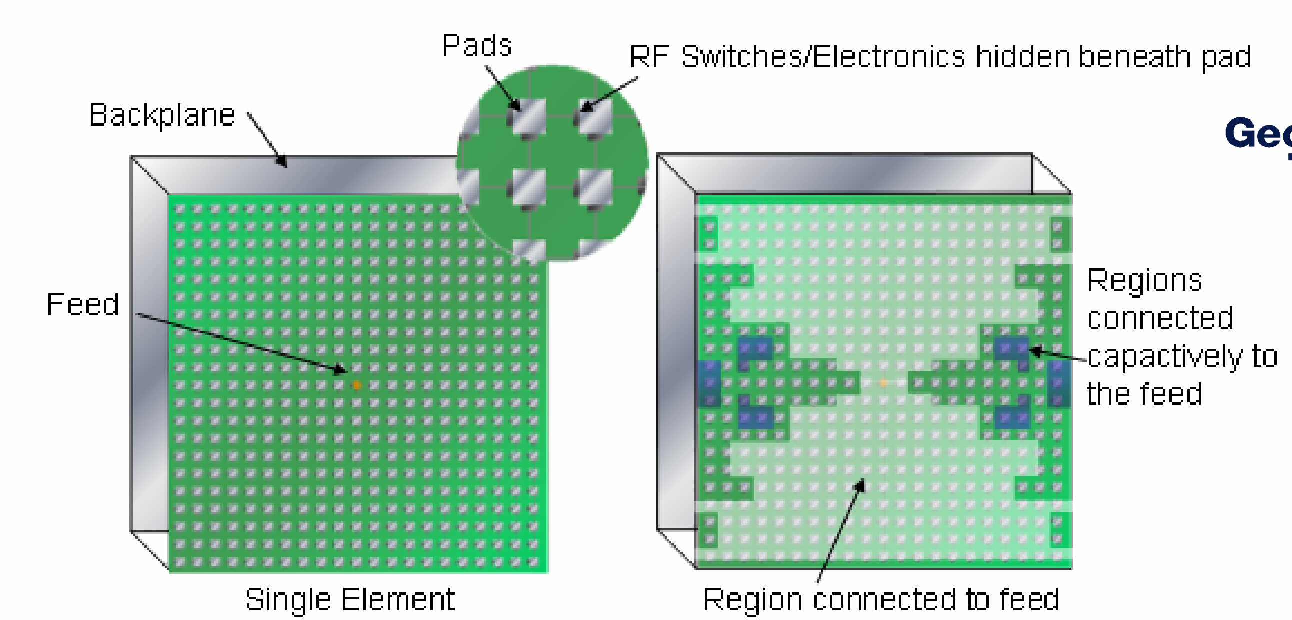
- **Embedded Control Electronics**
  - Utilizes a Honeywell electronics design solely driven by an optical interface
    - Optical backplane is composed of DSP controlled VCSEL array
    - ASIC development for the embedded aperture electronics
    - Power efficient economical solution with improved manufacturability



1.J. C. Maloney, M.P. Kesler, L. M. Lust, L.N. Pringle, T. L. Fountain, P. H. Harms, G.S. Smith, " Switched Fragmented Aperture Antennas", IEEE Antennas Propagat. Soc. Int. Symposium,, vol 1, pp. 310-313, July 2000.

ESCAN's Structural Form is Based on GTRI RECAP

- **The radiative pattern generated from a single feed element may be reconfigured by connective switches located between each pad.**
  - Individual pads<< λ and are not resonate alone
  - Collectively the pads connected to the feed generate a radiating form.
  - The parasitic pads capacitively coupled to the feed may be configured to improve matching characteristics enabling wider band performance.

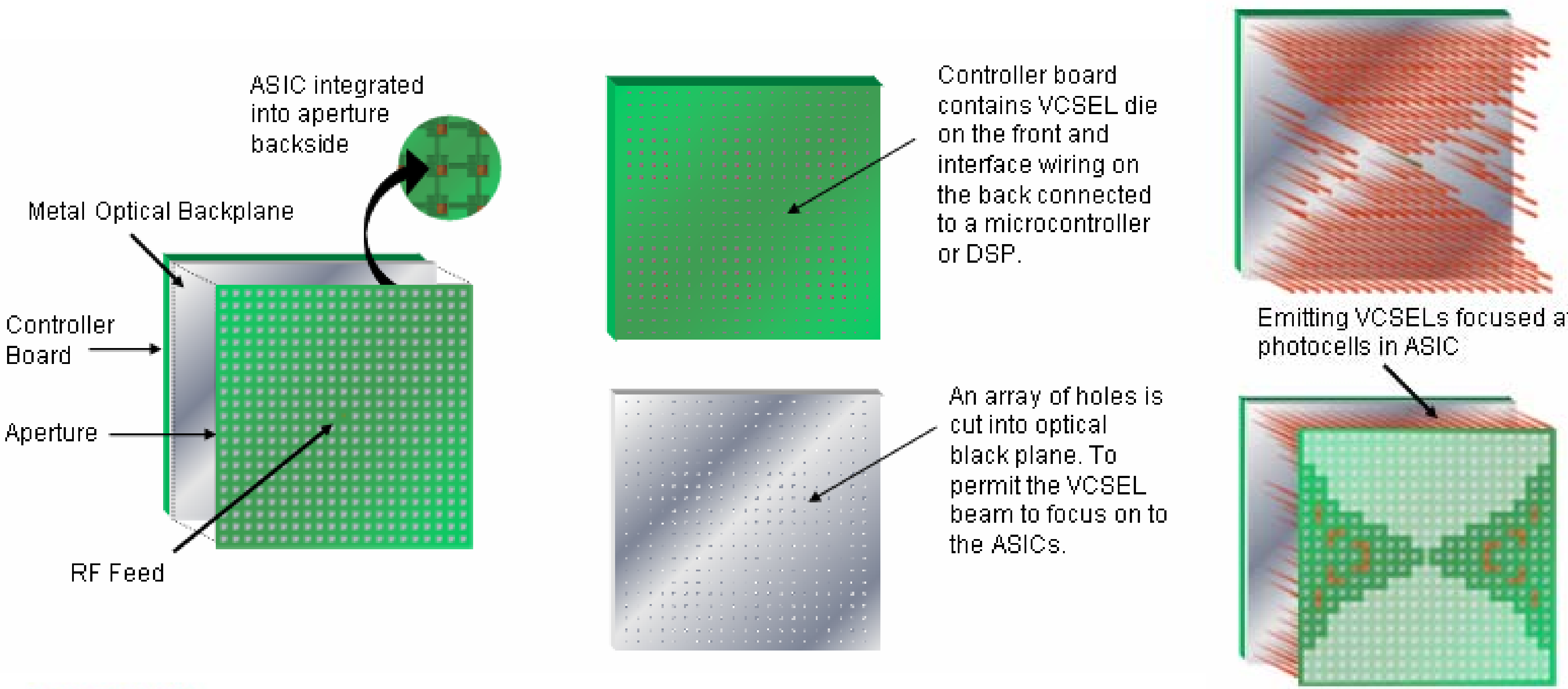


ESCAN: Design Rules of Thumb for the Structural Architecture

- **Pad Dimension: 1cm**
- **Pad Density $\lambda/7$ to $\lambda/11$**
  - Increased density permits broader beamsteering but forces higher switch density into the aperture.
- **Element Dimension 2λ x 2λ (25cm x 25cm)**
  - 20 x 20 pads (400 pads/element)
- **Array Dimension 5x1 (1.25m x 0.25m)**
- **Ground Plane Distance $\lambda/4$ @ 2.4 GHz (3cm)**

ESCAN: Honeywell's Embedded Controls

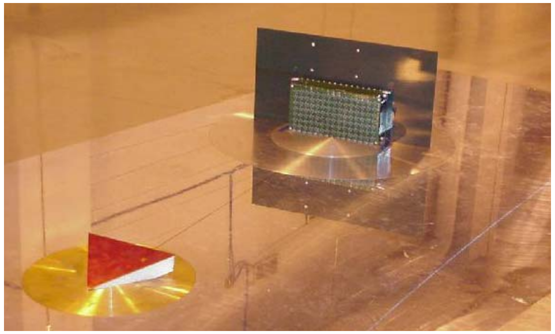
- **Power efficiency enables pure optical interface**
  - ASIC embedded behind each pad contains a photocell and RF switch
  - VCSEL array is situated on a PCB behind the antenna ground plane
  - VCSEL array is controlled by 1 DSP/microcontroller per element



ESCAN Measurement

ESCAN possess thousands of reconfiguration states posing a nontrivial measurement task.

Pattern cuts will be generated at the Georgia Tech Research Institute where automated ground plane and range testing has been developed for these specialized apertures.

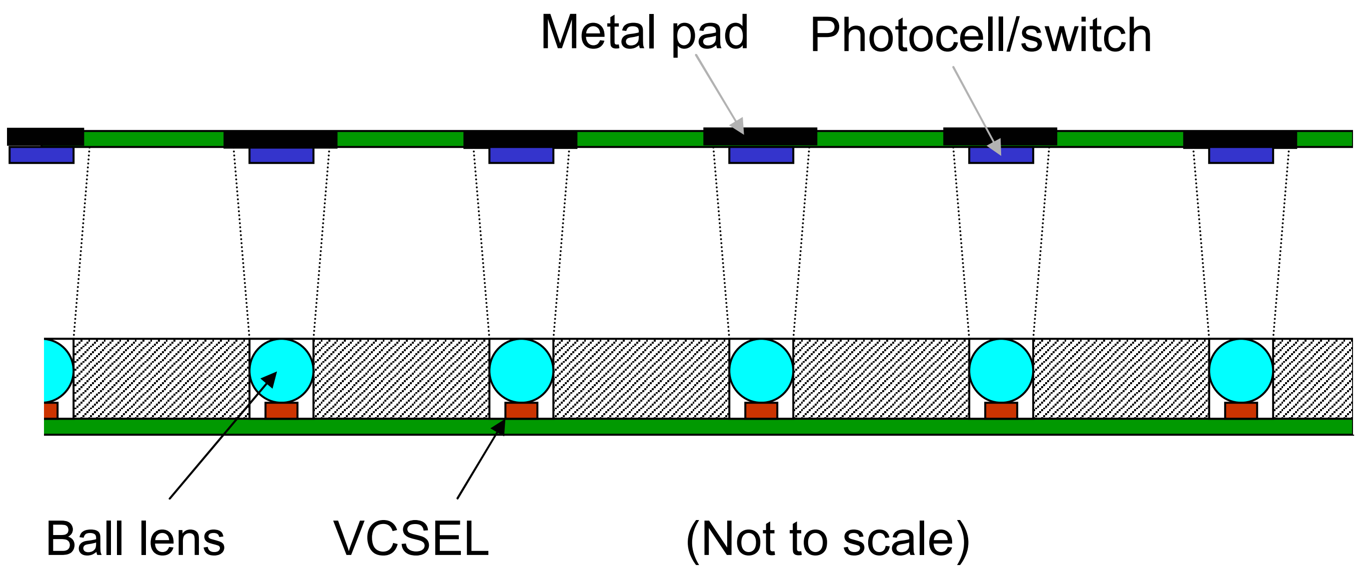


ESCAN Program Goals

- **Bandwidth: 800MHz -2.6GHz**
- **Element Broadside Gain: 13dB @ 2.4GHz and 7dB @ 900Mhz**
  - Theoretical Aperture Gain=$4\pi/\lambda^2$=17dB
- **5 x 1 Array Broadside Gain: 19dB @ 2.4GHz and 13dB @ 900Mhz**
- **Element Broadside Beamwidth: 32deg @ 2.4GHz 85deg @ 900MHz**
- **Array Broadside Beamwidth: 4.5deg @ 2.4GHz 12deg @ 900MHz**
- **Steering: +/-70 deg**
  - Controlled by pad density and the insertion form factor of the array
- **Power Handling: 1W CW per feed at 2.4GHz**
  - Switch dependent
- **Reconfiguration Time: 20 usec**
  - Dependent on photocell
- **Production cost: Significant reduction from electronically scanned arrays**
- **Ease of Manufacture**

ESCAN ASIC Development

- ASIC includes 2 RF switches and photodetector (PD)
- Switch insertion loss needs to be minimized and isolation maximized for good power handling and antenna gain
- VCSEL output is concentrated on photocell array to maximize photocurrent and switching speed



(Not to scale)

ESCAN VCSEL & Photocell Considerations

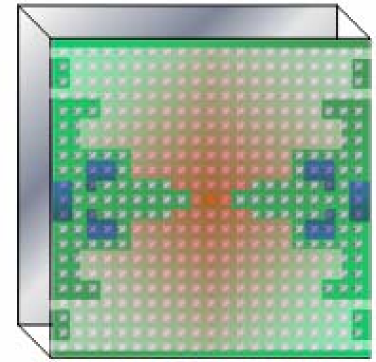
- **Honeywell Designed VCSEL SV5637-001**
  - 850nm wavelength
  - Beam divergence ~ 2 degrees
  - 1.1 mm spot diameter at photovoltaic cell
  - Output power 1.5 mW

- **11 Cell GaAs Process**
  - Photovoltaic cell area 11 x 0.085 mm^2
  - Power received ~136 μW
  - 10^{17} n-doping photovoltaic cell (92 pF, ~68 μA photocurrent@ ~0.8volts)
  - Switching time ~ 1 μs

- **18 Cell Silicon CMOS Process**
  - Photovoltaic cell area 18 x 0.052 mm^2
  - Power received ~83 μW
  - 10^{17} n-doping photovoltaic cell (67 pF, ~30 μA photocurrent@ ~0.5volts)
  - Switching time ~ 1.2 μs

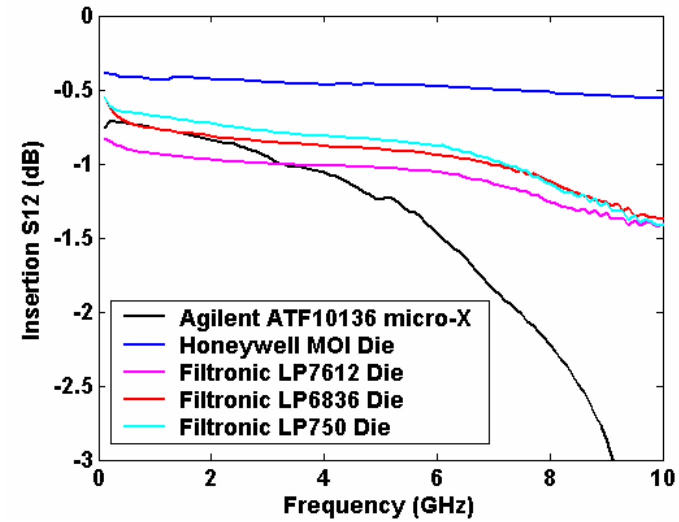
ESCAN Switch Design Considerations

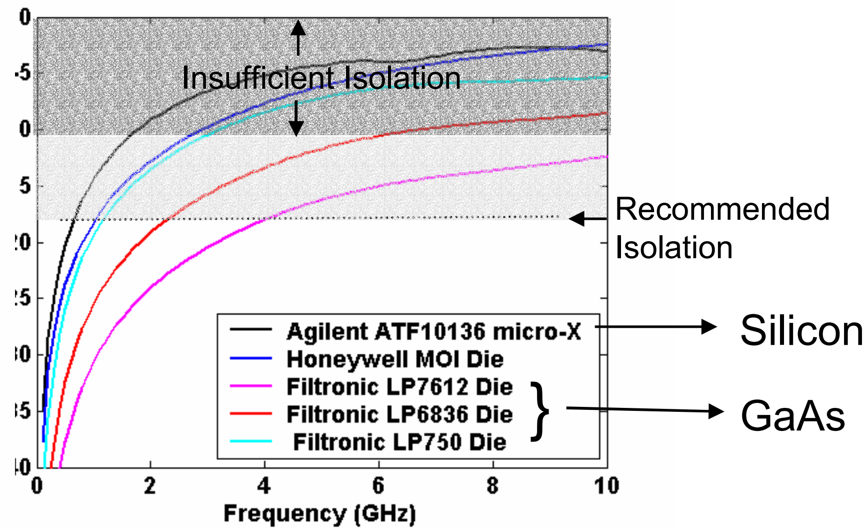
- **Insertion loss (IL) and Isolation**
  - Low IL and high isolation designs diametrically oppose
  - Insertion loss determines the physical extent of the element
  - Increasing insertion loss gradually degrades the realized gain continuously (target <1 dB)
  - Decreasing the isolation induces an abrupt change in the element performance (target < -11dB)



High Insertion Loss
Currents attenuated at edges

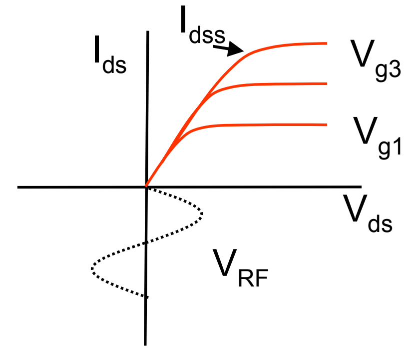
2001 Switch Data





ESCAN Power Handling Considerations

- **FET Power Handling**
  - **ON State**
    - $I_{pk} > I_{DSS}$ compression results
    - Max Power (On State) $= 0.5 * \left(I_{dss\_max}^{2} Z\right)$



  - **OFF State**
    - At RF frequencies V_g moves in sync with the RF swing on the drain (buys a factor of 2)
    - Compression results when V_{RF} causes the V_{gd_max} to be exceeded

$$V_{RF} = 2\left(V_{dg\_max} - V_g\right)$$

    - When V_{RF} forces the FET beyond pinch off

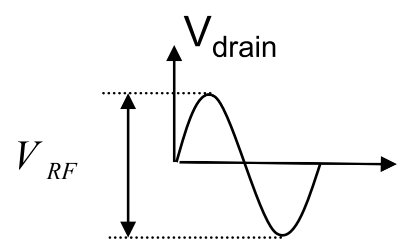
$$V_{RF} = 2\left(V_p - V_g\right)$$

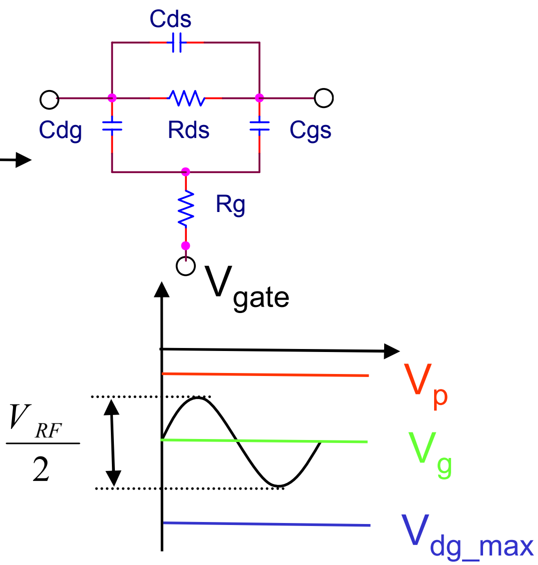
    - Optimum gate voltage

$$V_g = 0.5 * \left(V_p + V_{dg\_max}\right)$$

    - Max Power (Off State)

$$= 0.5 * \left(V_{dg\_max} - V_p\right)^2 / Z$$





ESCAN Power Handling Estimates

- **FET Power Handling**
  - **Typical Values**
    - Vdg_max=-16 V;
    - Vp=-1.2 V;
    - Vopt_gate = -8.6 V;
    - Idss = 115mA @ Vg=0
    - Utilizing a positive gate voltage to increase Idss to Idssmax~ 1.5*Idss ~ 175mA
    - Max Power (Off State) ~ 2.2-1.1 Watt (for Z=50Ω-100Ω)
    - Max Power (On State) ~ 0.77-1.53 Watt (for Z=50Ω-100Ω)

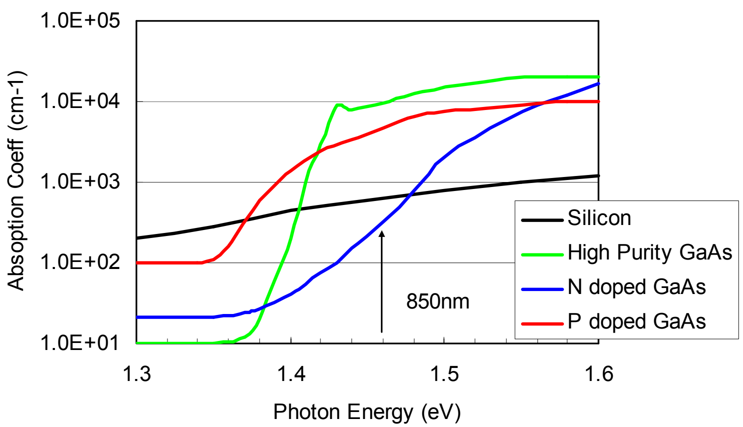
ESCAN ASIC Process Selection Summary

GaAs

- 850nm P-doped GaAs PD is most efficient
- Operation req. 11 ~0.9V Voc stacked PDs
- 300 micron FET switch has ~ 1.0 dB IL and 23 dB isolation at 2.4GHz
- GaAs substrates have low loss
- ESD protection is not required
- Logic not available
  - 2 ASICs & VCSELs per pad
- P doped GaAs is not readily available

Silicon

- 850nm PD operation is less efficient
- Operation req. 18 ~0.5V Voc stacked PDs
- 300 micron NMOS SOI switches has ~ 1.0 dB IL and 19 dB isolation at 2.4GHz
- Si substrate degrades isolation and IL
- ESD protection req.
- CMOS logic circuits reduce VCSEL count
  - 1 ASIC & VCSEL per pad
- Process is readily available



Performance vs. Cost

ESCAN Summary

- **ESCAN: 5x1 Array with a 20 pad x 20 pad element**
- **Performance:**
  - Bandwidth: 800MHz -2.6GHz
  - 5 x 1 Array Broadside Gain: 19dB @ 2.4GHz
  - 1-5 Independent Beams
  - Steering: +/-70 deg
  - Power Handling: 1W CW per feed at 2.4GHz
  - Reconfiguration Time: 20 usec
- **Depending on phased array performance electronically scanned arrays range between $100K - $300K. ESCAN production costs are 1-2 orders of magnitude LESS regardless of the process utilized.**